SONY CXD1225M

Frequency Synthesizer PLL

T-50-17

Description

CXD1225M are used for the digital selection of TV broadcasting as well as AM, FM and various radio waves. These PLL IC's were developed through high speed N-channel silicon gate MOS technology.

Features

- The maximum operating frequency is guaranteed as follows.
  CXD1225M } 300MHz
  Usage up to 1 GHz is possible when combined with an ECL (general purpose) prescaler.

- Programmable divider permits the division of a program frequency up to 1/262, 151
- Programmable reference divider permits the selection of comparison frequency at will.
  (E.G. Using a 4MHz crystal oscillator selection from 244Hz to 2MHz is possible)
- High-speed phase comparator provides high C/N ratio.
- Operation control through 3pins.
- 3 independent pins (AM1, FM1, TV1) are provided for the signal input at respective frequencies.
- Multipurpose output terminals are provided (A0, B0)
- Low consumption (Standard: 120W)

Structure

N-channel silicon gate MOS

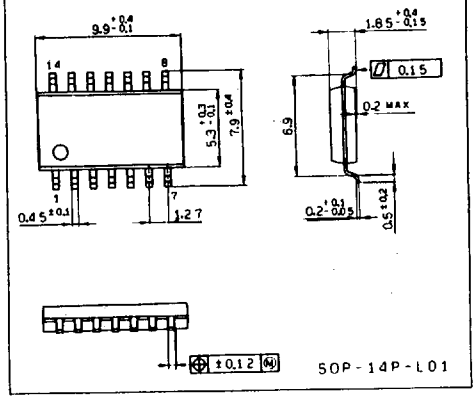
Absolute Maximum Ratings (Ta=25°C, Vss=0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Input pin voltage	V_{IN}	−1 to +7	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Starage temperature	T_{stg}	−55 to +150	°C

Package Outline

Unit: mm

CXD1225M 14pin SOP (Plastic)



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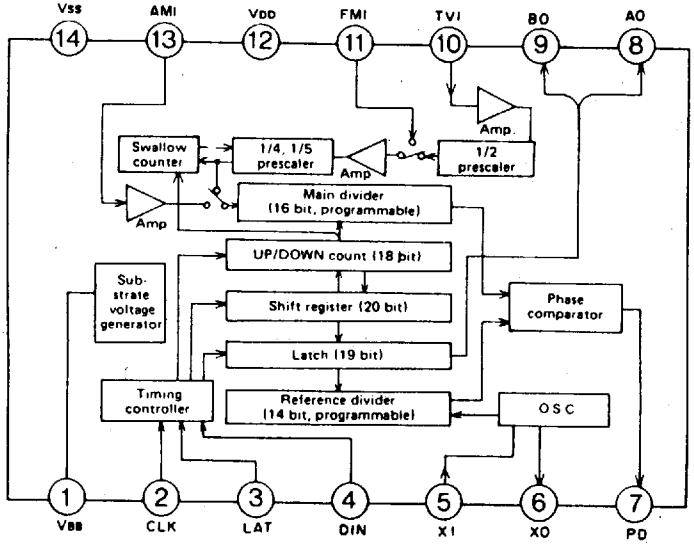
Recommended Operating Conditions

Item	Pin Remarks	Symbol	Operating range	Unit
Supply voltage		V_{DD}	+4.5 to +5.5	V
High level input voltage	CLK, DIN LAT	V_{IH}	+2.6 to V_{DD} +0.5	V
Low level input voltage		V_{IL}	−1.0 to 0.8	V
High frequency signal input amplitude	TVI	e_{IN}	0.3 to 4.0	Vp-p
High frequency signal input amplitude	FMI	e_{IN}	0.2 to 4.0	Vp-p
High frequency signal input amplitude	AMI	e_{IN}	0.2 to 2.5	Vp-p
High frequency signal input amplitude	XI	e_{IN}	0.6 to 4.0	Vp-p
Operating temperature		Topr	−20 to +70	°C

Block Diagram and Pin Configuration



Pin Description

No.	Symbol	Description
1	V_{BB}	Substrate pin. (Connect 0.01μF capacitor between this pin and GND)
2	CLK	Clock input pin for 20bit serial data input.
3	LAT	Latch signal input pin for shift register input data (latched with signal rise) Also, Up/Down clock input pin (state changes with signal rise)
4	DIN	Data input pin. Also, Up/Down mode select pin (Up at 'H' level, Down at 'L' level)
5	XI	Crystal oscillator connection pin for reference signal generation. (Max. 13MHz Standard 4.0MHz)
6	XO	
7	PD	Phase comparator output pin (3States)
8	AO	External control signal output pin/unlock output pin (E/E MOS push-pull)
9	BO	External control signal output pin/data check pin (E/E MOS push-pull)
10	TVI	High frequency signal input pin (Max. 300MHz) 1/2 prescaler built-in.
11	FMI	High frequency signal input pin (Max. 150MHz)
12	V_{DD}	Supply (+5V)
13	AMI	High frequency signal input pin (Max. 40MHz)
14	V_{SS}	Ground pin

Electrical Characteristics

(Within Recommended Operation Conditions range, unless otherwise specified) Vss=0V

Item	Pin, Remarks	Symbol	Conditions	CXD1225M			Unit
				min.	Typ.	Max.	
Operating supply current	V_{DD}	I_{DD}	Note2		24	40	mA
Operating input frequency	TVI	f_{OP}	e_{IN}=0.3 to 4.0Vp-p	20		300	MHz
	FMI	f_{OP}	e_{IN}=0.2 to 4.0Vp-p	20		150	MHz
	AMI	f_{OP}	e_{IN}=0.2 to 2.5Vp-p	0.05		40	MHz
Input leak current	Logic input	I_{IL}	V_{IH}=0 to VDD Note1	-10		+10	μA
High level output current	Phase comparator (3 value output) PD	I_{OH}	V_{OUT}=3V Note2			-0.2	mA
Low level output current		I_{OL}	V_{OUT}=1V Note2				mA
High impedance leak current		I_{HZ}	V_{OUT}=2V Note2	+0.2		+50	nA
High level output voltage	Push-pull by E/E MOS: Composition AO, BO	V_{OH}	I_{OH}=-20μA	-50			V
Low level output voltage		V_{OL}	I_{OL}=-1mA	2.8		0.6	V

Note 1) Ta=25°C

Note 2) V_{DD}=5V Ta=25°C

Operating Input Frequency Test Circuit

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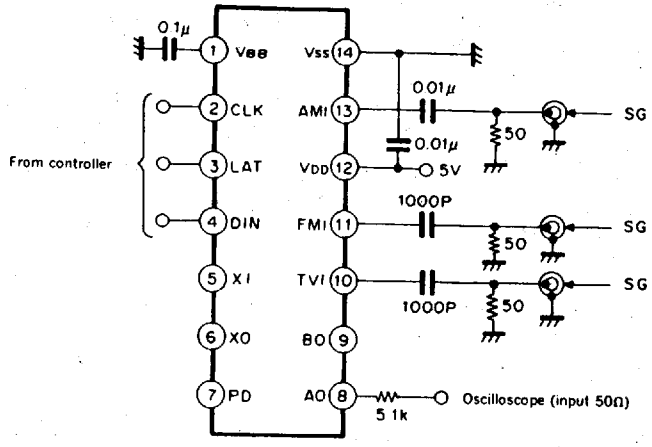


Control input data to CX-7925B/CXD1225M: T1-H, T2-H, A-L, B-H
SG: HP's 8640B
(Input level read directly at built-in level meter)

Operation

[1] Signal input from the local oscillator

CXD1225M use 3 independent input pins according to frequency and application.

- AMI pin

  Reception pin for AM and TV broadcast. Signal input up to 40MHz is warranted for CXD1225M. Frequency division ratio when using this pin is 1/2 to 1/65537.

- FMI pin

  Reception pin for FM and TV broadcast. Signal input up to 150MHz is warranted for CXD1225M. Accordingly, the external prescaler is not required for FM reception. For TV reception, the entire TV band width can be overed through combination with an external prescaler up to 1/8. Frequency division ratio ranges from 1/12 to 1/262151. When not in use this pin stays open.

- TVI pin

  This pin is solely used for TV broadcast reception. With the built-in 1/2 prescaler signal input up to 300MHz is warranted for CXD1225M. The entire bandwidth can be covered through combination with an external prescaler up to 1/4. Frequency division ratio ranges from 1/24 to 1/524302. When not in use this pin is grounded internally via a resistor of more than 100kΩ.

[2] Phase comparator output

The phase comparator output (PD pin) has a 3-level value. The pin is at High level when the input signal is more aduanced in phase than the reference signal. At Low level when the phase lags behind and at high impedance when they are in phase.

[3] Control signal and control system

CX-7925B/CXD1225M are designed as controllers compatible with general 4 or 8-bit microcomputers. There are 3 control input pins CLK, LAT, DIN and 2 control output pins AB and BO. Through the proper combination of these pins, the simplification and multi-functionalization of the system can be realized.

CX-7925B/CXD1225M feature 3 data input modes, (normal mode), Up/Down mode and Data check mode with different signal input patterns for each.

(3-1) Control signal input modes

(a) Data input mode (normal mode)

To set all initial values of CXD1225M a total of 40bit of data has to be input 20bits at a time. With LAT pin at Low, as data is input to DIN pin, data is input to the shift register 1 bit at a time with the rising edge of the clock input to CLK pin.

After 20bit of data has been transmitted to the shift register, with CLK at High as LAT pin is set to High, data is latched, (after data is latched, turn LAT pin back to Low, Varying DIN and CLK pins while LAT pin is at High may affect data internally).

As will be described in detail later on, input data is input either in the programmable divider or the reference divider according to the state of the last bitC. In practice input from the controller the 20bit of the data including first the reference divider frequency, input pin selection and AO, BO output pins data using the above methed. Here the data last bit is set to Low.

Next input 20bit including data used to set the programmable divider, in the same way. Here set the last bitC to High. This sets all internal states. After that, to vary only the programmable divider value, varying only the latter 20bit of data will suffice (In this case too, C is to be set to High).

To vary the programmable divider value (channel selection, AFT) the usage of Up/Down mode mentioned hereafter will improve efficiency.

(b) UP/DOWN mode

After setting CLK pin to Low, the contents of UP/DOWN counter can be increased or decreased by one according to DIN pin High, Low level. This by turning LAT pin (normally at Low level) from High to Low. By repeating this process the setting value of the programmable divider can be varied as required.

(c) DATA CHECK mode

This mode is used to check if data has been correctly input from the controller to the data register. Data left in the shift register immediately after input data has been latched is output bit by bit from BO pin. This at the rising edge of a clock input pin and at to CLK pin while it is held to High and after LAT pin is set to Low. The shift register data can only be output from BO pin when bits T1 and T2 of the data are at High and Low, respectively.

(3-2) Control data assignment

CZD1225M is assigned in 20bits. The last 20bits are the data identification code. Identifying the code will tell the data contents. Though unrelated to users, switching to Test mode is also performed using this code. Each of the programmable divider and reference divider frequency number is given in binary value with LSB at the leading digit.

(a) Control input data of the Reference divider (C=Low)

This can be described as the initialization setting data. It is always input when power is fed or when a channel band is switched. The input data composition is as follows.

R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	PI1	PI2	A	B	T1	C

LSB MSB

- R0 to R13 ; Reference divider frequency division numbers. (binary value with R0 as LSB)
  There is an offset element between the input data and the actual frequency division numbers. The relationship being (actual frequency division numbers)=(Input data+2)
- PI1, PI2 ; Specification of the signal input pin.

Input / PI1, PI2	AMI	FMI	TVI
PI1	—	L	H
PI2	L	H	H

• A, B, T1 ; Each of AO and BO pins features 2 functions selected according to T1 value. When T1 is at Low, A and B values are output as they are to AO and BO pins. These signals can be used to select the prescaler frequency division, the filter constant, the channel band signal and various other purposes. When the prescaler M54465P (mitsubishi) for TV reception is used the following selection codes for frequency division ratio apply.

Frequency division ratio / A, B	1/2	1/4	1/8
A	H	L	L
B	L	H	L

When T1 is at High, AO output pin outputs the phase comparator LOCK/UNLOCK state.
AO pin H; UNLOCK
L; LOCK
BO pin becomes, as described in Paragraph[3-1]C for Data check mode, the shift register data output pin. Through the clock input to CLK pin the shift register content is continuously output. Note that when T1 is at High, AO and BO pins can not be used for external control.

• C ; This code determines the latch direction of the input data. In this case, set to Low.

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output
H	H	L	H	Main divider output	

(b) Programmable divider input data (C=High)
This data determines the Programmable divider frequency division ratio.

N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	T2	C

LSB MSB

• N0 to N17; Programmable divider frequen division numbers. (Binary value with N0 as LSB) The actual frequency division number differs according to the pin selected for the signal input as follows.

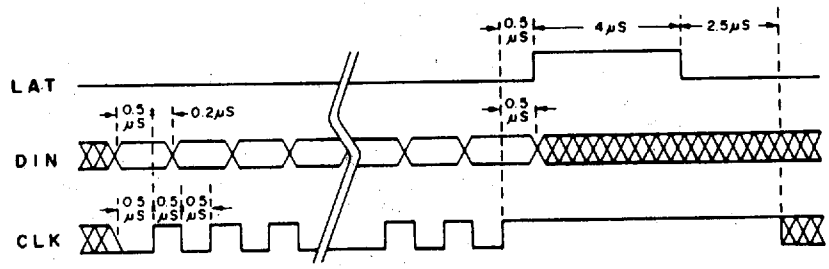
Control data		Input pin	N frequency division input data range	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
PI1	PI2				
—	L	AMI	0 to 65535	N+2	2 to 65537
L	H	FMI	4 to 262143	N+8	12 to 262151
H	H	TVI	4 to 262143	2 • (N+8)	24 to 524302

- T2 ; T2 is used for Test mode selection. Users usually set this data to Low. To test the frequency division output and reference output this T2 bit and afore mentioned T1 bit are set to High while A and B bits are set to Low. Then, a reference output and a frequency division output can be observed at AO and Bo pins respectively.
- C ; As described before, set to High in this case.

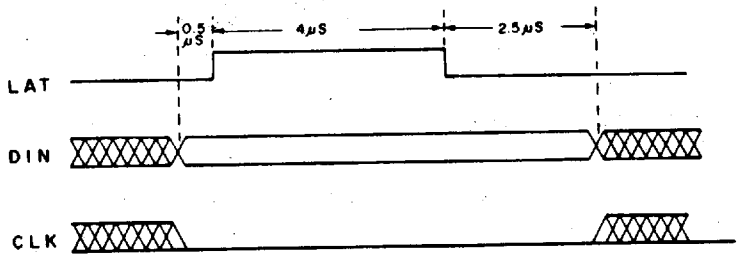
[3-3] Data input and control signal timing

(a) Data input mode (normal mode)

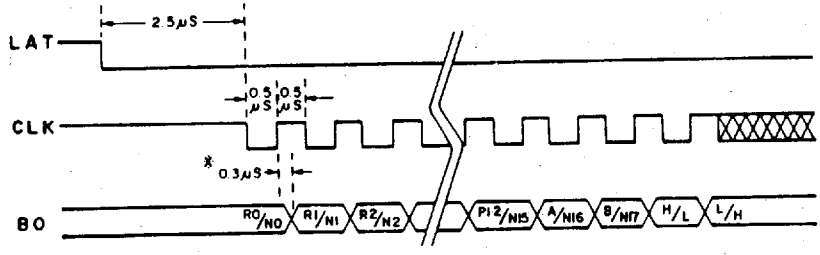
Various timings show the minimum value unless otherwise indicated.



(b) UP/DOWN mode



(c) DATA CHECK mode (Shift register data check)



(* Mark indicates data is output within this timing)

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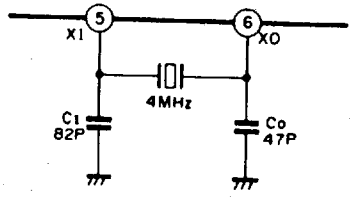
[4] Reference signal (Reference divider input signal)

The connection of a chrystal oscillator to X1 and X0 allow these IC's to generate reference signals. The input of an external clock signal to X1 pin permits the usage of an external clock as reference signal.

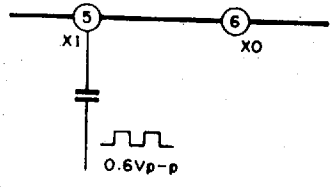
[4-1] Reference signal generation by means of built-in oscillator

Connect a chrystal oscillator with a frequency of 1MHz to 13MHz to X1 and X0 pins, as shown below. The diagram below shows an example where a standard 4MHz osillator is used. The capacitance ratio of C_1, C_0 should be 1 to 2 : 1 while their serial capacitance values should be the specific load capacitance of the chrystal oscillator.

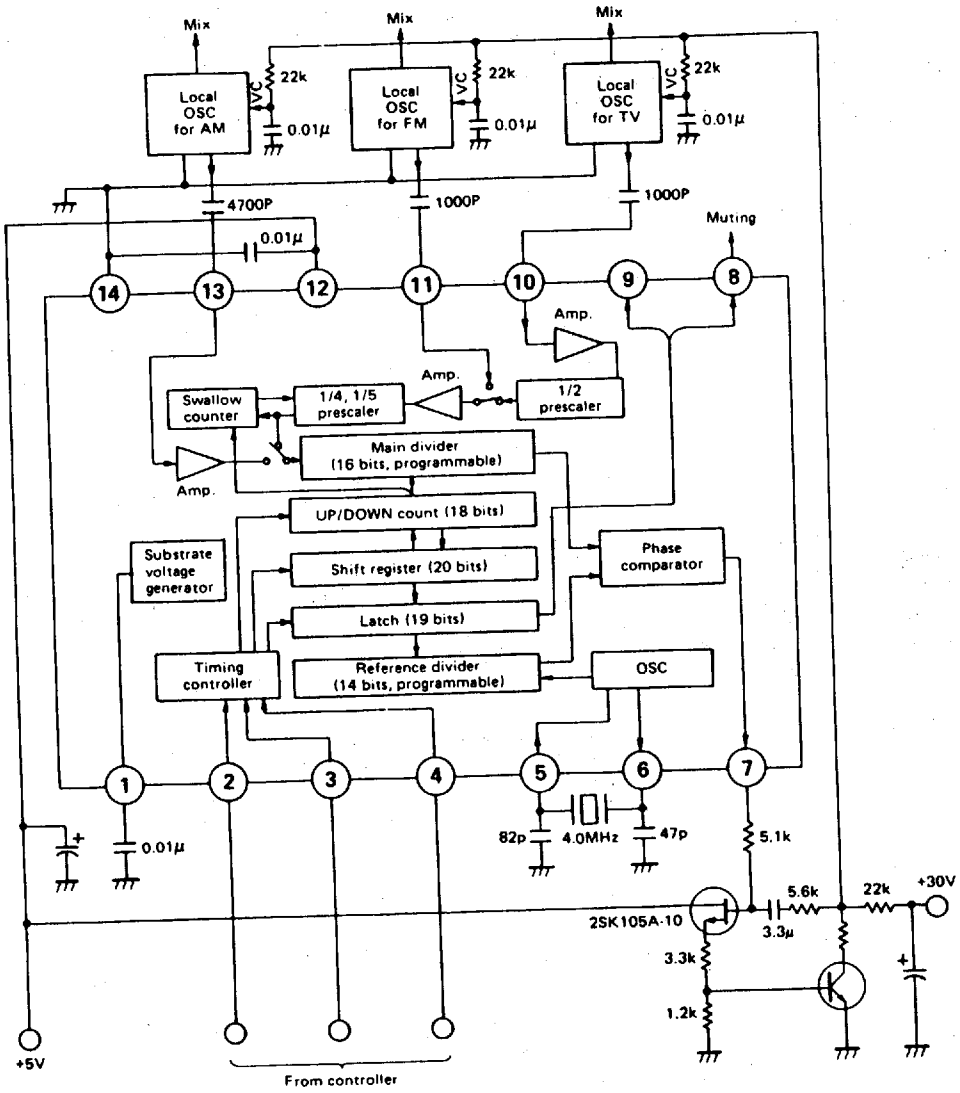


[4-2] Reference signal generation by means of external clock

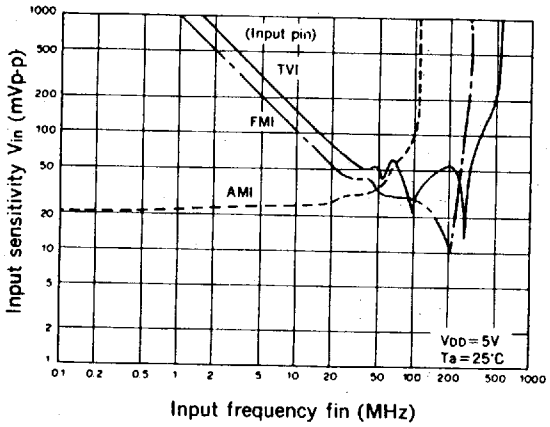
When an external clock signal, such as a clock signal obtained from the controller is to be used as reference clock, input it to X1 pin via a capacitor as shown below. The clock frequency range is guaranteed up to 13MHz. However, the usage of a signal with proper rise and fall (over 5V/μs) is recommended especially when the frequency is low. This is to prevent malfunction.



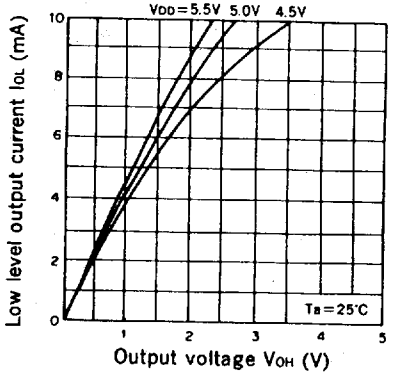
Application Circuit

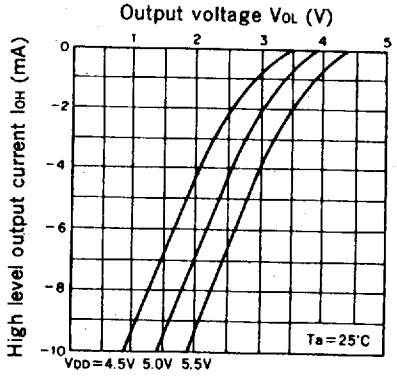


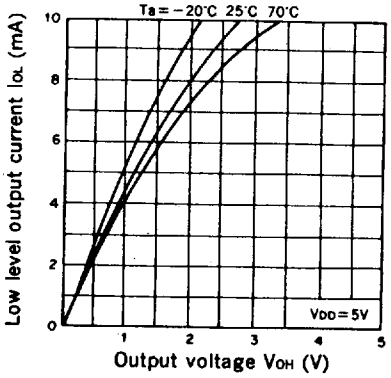
High Frequency Input Sensitivity Characteristics

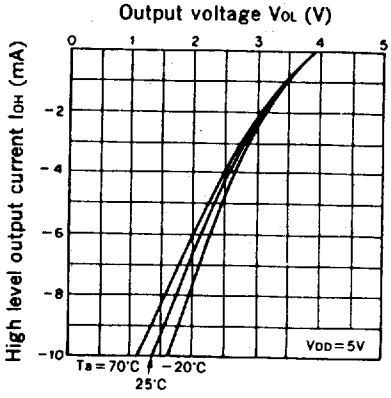


AO, BO pins Output Current Characteristics

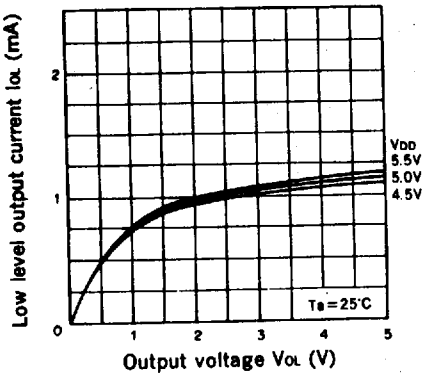


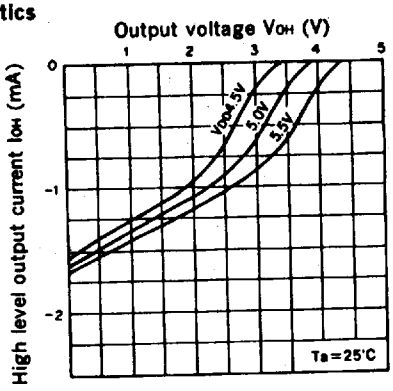


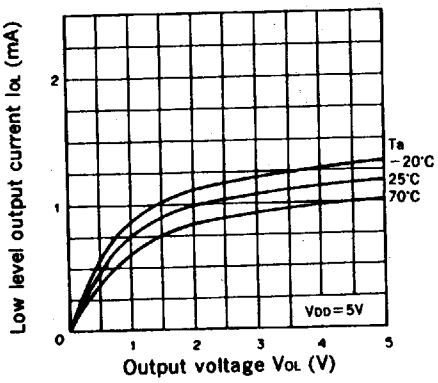


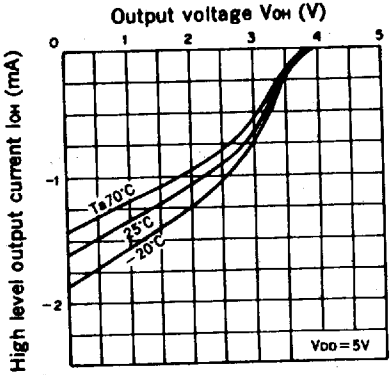


PD (Phase Comparator) pin Output Current Characteristics









Supply Current I_{DD} and Voltage Characteristics